

ABSTRACT OF THE DISCLOSURE

An aspect of the present invention provides a
5 microprocessor that includes a processor core including an
instruction executing unit configured to execute instructions
for input and output controlling and processing for data and
a cache memory configured to store the data, a memory
management unit coupled to the processor core, the memory
10 management unit configured to manage memory system including
the cache memory, and a bus interface coupled to the processor
core and the memory management unit, the bus interface
configured to rearrange the bits of the data transferred from
the processor core.